halt execution. This usually involved a chip that had more pins than the production device (an SE or special emulation device). This analysis model does not work well in the System-on-a-Chip (SOC) era as the integration levels and clock rates of today's devices preclude full visibility bus export.--

Rewrite the paragraph at page 15, lines 10 to 19 as follows:

--Advanced analysis provides affordable on-chip instruction and data bus comparators, sequencers and state machines, and event counters to recreate the most important portions of the triggering function historically found off chip. Advanced analysis provides the control aspect of debug triggering mechanism for Trace, ~~RTDX~~ RTDX™ and Real-Time Emulation. This architectural component identifies events, tracks event sequences, and assigns actions based on their occurrence (break execution, enable/disable trace, count, enable/disable ~~RTDX~~ RTDX™, etc.). The modular building blocks for this capability include bus comparators, external event generators, state machines or state sequencers, and trigger generators. The modularity of the advanced analysis system allows the trade off of functionality versus gates.--

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Rewrite the paragraph at page ~~18~~ 19, line 5 as follows:

--• ~~RTDX~~ RTDX™;--

Rewrite the paragraph at page 19, lines 12 to 17 as follows:

--The emulation controller 12 accesses Real-time Emulation capabilities (execution control, memory, and register access) via a 3, 4, or 5 bit scan based interface. ~~RTDX~~ RTDX™ capabilities can be accessed by scan or by using three higher bandwidth ~~RTDX~~ RTDX™ formats that use direct target-to-emulator connections other than scan. The input and output triggers allow other system components to signal the chip with debug events and vice-versa.--